SBC84500 Series

3.5” HDD Form Factor
SBC with CRT/TFT/AUDIO
and Fast Ethernet

User’s Manual

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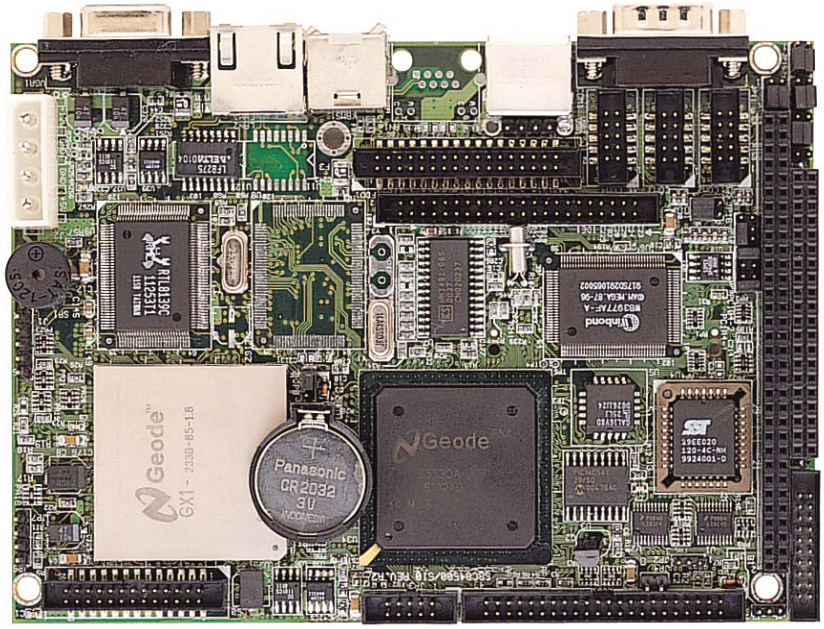
Chapter 1
Introduction

1.1 General Description



AXIOMTEK new SBC84500 NS Geode Series is a 3.5" SBC which offers an onboard NS Geode GX1-233 processor, plus support for Ethernet network functions onboard features include VGA/TFT LCD, a Compact-Flash™ card socket, and watchdog timer. With the 586-level NS Geode processor mounted directly on board, upgrade and system configuration is much more convenient as is the benefits of fan less operation in temperatures up to 60° C (140° F). This board is a feature-packed, 586-level, hassle-free solution for space critical applications.

The SBC84500 Series complies with the "Green Function" standard and supports three types of power saving features: Normal, Doze, and Sleep modes. The display type configuration is done through software. A single Flash chip holds the system BIOS and the VGA BIOS. This minimizes the number of chips and eases configuration. You can change the display BIOS simply by programming the Flash chip. If you need any additional functions, the SBC84500 Series has a PC/104 connector for future upgrades.

1.2 Specifications

Process:	233MHz National Semiconductor Geode GX1 (other frequency processors are manufacturer optional)
Chipset:	NS GX1 + CS5530A
Memory:	1x144-pin SODIMM Max. 256MB SDRAM (Please refer to **Appendix C** for more information.)
On-board IDE:	PIO Mode 0-4, DMA Mode 0-1 and One Channel up to 2 Devices (44-pin Box-header) Enhanced IDE ATAPI/16.6/33,LS-120 Bootable
On-Board Multi I/O:	One Floppy Port(Box-header) Supports up to 2 Device (LS-120 Bootable) One SPP/EPP/ECP Parallel Port(Box-header),(LS-120 Bootable) Four 16550 UARTs Compatible Serial Ports with +5V/+12V Power Output in Pin 1(+5V) and Pin 9(+12V) via Jumper Setting: 1 x RS-232 (COM1 as D-type) 1 x RS-232/422/485 Jumper Selectable (COM2 Box-header) 2 x RS-232 (COM3/4 Box-header) One IrDA (Pin-header) for Wireless Communication
PS/2 KB /MOUSE:	PS/2 Type (Mini-Din Connector)
Watchdog Timer:	System Reset Software Programmable Timer Interval 64 Levels, 0.5~8 / 5~80 / 50~800 / 100~1600 Seconds

BIOS:	AWARD BIOS with DMI, Plug-and-Play
	& Y2K Compliant in 2Mbit Flash Rom
	SmartView VGA BIOS Function
	Integration Ethernet Novell Boot Rom Function
RTC:	Integration in W83977AF with external Lithium Battery
On-Board Display:	CS5530A South Bridge Integrated Support CRT/TFT Display via UMA Max. to 4MB Sharing Memory
	Resolution ~Non-interlaced CRT and TFT Monitor up to 1024 x 768 @ 64K Color
On-Board Ethernet:	Realtek 8139C PCI PnP 10/100Base-T Ethernet
On-Board Audio:	AC97 Codec with Surround Sound
	Microsoft Direct Sound 3D Audio Supported
	32-bit Sound Blaster TM and Sound Blaster TM Pro Compatible
	Full-duplex Operation for Simultaneous Record and Playback
	Internal MIC-in, Line-in and Speaker-out interface Reserved
On-Board SSD:	CompactFlash™ Socket
Extension:	One 16-bit PC/104 Connector
Power Supply:	Single +5V(Range: 4.75~5.25V)
	(Please refer to **Appendix B** for more information.)
	Internal Power Connector (+5V, GND, GND, +12V)

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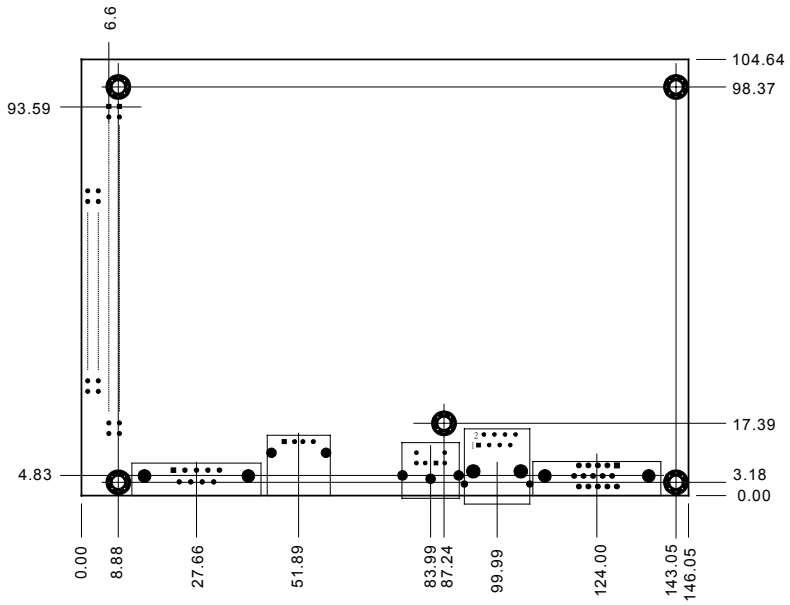
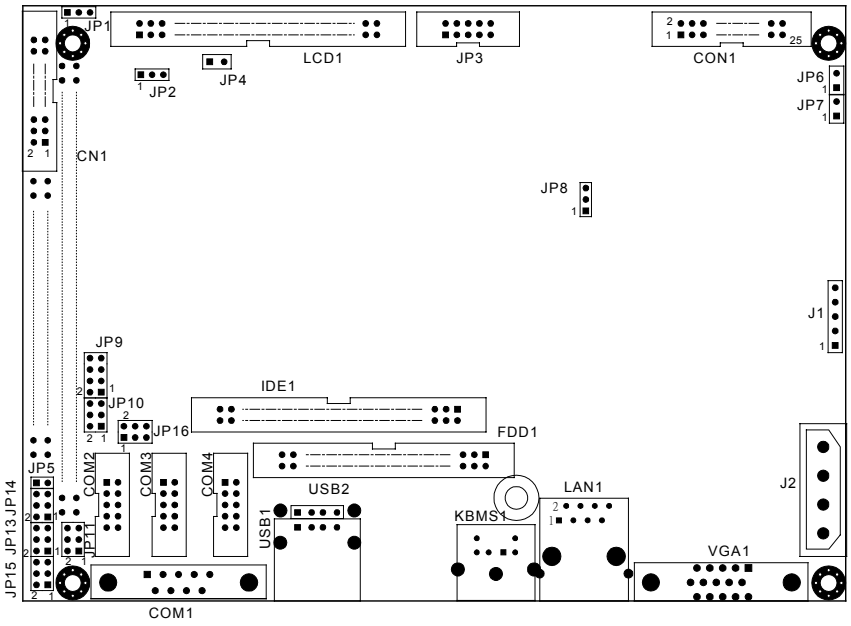
Chapter 2
Installation

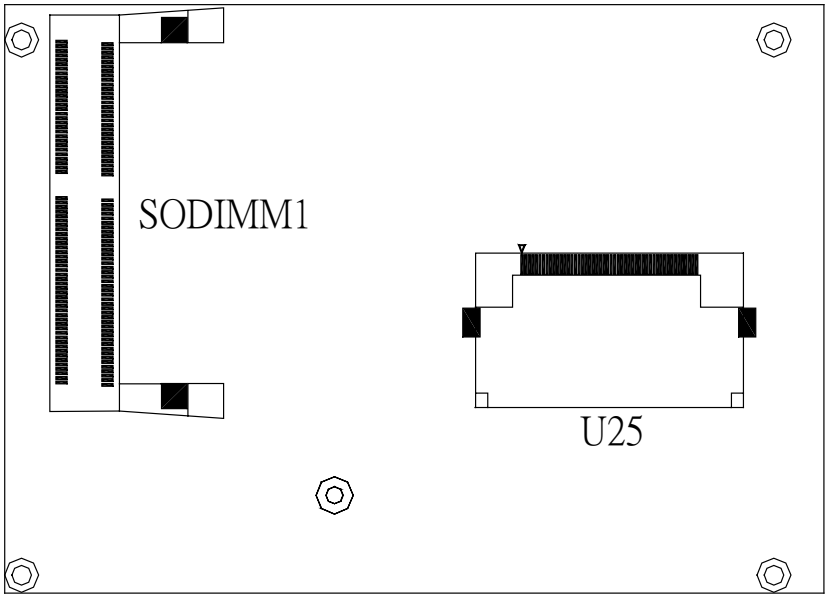
2.1 Board Dimension and Fixing Holes



Unit:mm

2.2 Placement





2.3 Jumper Settings

The SBC84500VEA is configured to match the needs of your application by proper jumper settings. The following tables show the correct jumper settings for the onboard devices.

Jumper	Default Setting	Jumper Setting
JP1	Watchdog Trigger Disabled	Open
JP2	Flat Panel Connector Voltage Selection: **Flat Panel Signal Level at 5.0V**	Short 1-2
JP5	Compact Flash IDE Mode for Master/Slave Selector Setting: **Slave**	Open
JP8	Clear CMOS Jumper: Normal	Short 1-2
JP9	COM2 RS232/422/485 Settings: RS-232	Short 1-2
JP10	COM2 RS232/422/485 Settings: RS-232	Short 3-5, 4-6
JP11	COM2 RS232/422/485 Settings: RS-232	Short 3-5, 4-6
JP13, JP15 JP14, JP16	Serial Port with +5V/+12V Power Setting	Short (3-5,4-6)

2.3.1 Watchdog Function Setting: JP1

The watchdog timer is an indispensable feature of the SBC84500VEA. It has a sensitive error detection function and a report function. When the CPU processing comes to a halt, the watchdog can generates a resets the CPU.

Watchdog Function	Settings
Reset system when Watchdog triggered	Short 2-3
Disabled	Open (default)

2.3.2 Serial Ports Settings: JP9, JP10, JP11

The SBC84500VEA provides 4 onboard serial ports, 3 x RS-232 and 1 x RS-232/422/485. The corresponding jumper settings are shown on the following table.
If COM2 is to be set to RS-422/485, the following jumpers have to be set correctly.

Options	Settings		
	JP9	JP10	JP11
RS-232 (default)	Short 1-2	Short 3-5, 4-6	Short 3-5, 4-6
RS-422	Short 3-4	Short 1-3, 2-4	Short 1-3, 2-4
RS-485	Short 5-6, 7-8	Short 1-3, 2-4	Short 1-3, 2-4

2.3.3 CMOS Clear Jumper: JP8

Options	Settings
Clear CMOS	Short 2-3
Normal	Short 1-2 (default)

2.3.4 Flat Panel Connector Voltage Selection: JP2

SBC84500VEA supports +3.3V or +5V for flat panel connector, with voltage selection completed by setting: **JP2**

V_{DDM} of LCD1 connector	JP2
5 V	Short 1-2 (default)
3.3 V	Short 2-3

2.3.5 Compact Flash IDE Mode Selection: JP5

SBC84500VEA Compact Flash IDE Mode for Master/Slave selection completed by setting: **JP5**

CF IDE Mode	JP5
Master	Short
Slave	Open (default)

2.3.6 Serial Ports +5V and +12V Power Selection: JP13, JP15, JP14, JP16

The four COM ports have +5V/+12V power capability on Pin 1 (+5V) and Pin 8 (+12V) or Pin 9 (+12V), depending on the jumper selection. The RS-232's pin assignments are listed.

JP13 (COM1), JP15 (COM2), JP14 (COM3), JP16 (COM4)

JP13, JP15, JP14, JP16	COM1	COM2	COM3	COM4	Description
Short 3-5 (default)	Pin 1	Pin 1	Pin 1	Pin 1	Data Carrier Detect (DCD)
Short 4-6 (default)	Pin 9	Pin 8	Pin8	Pin 8	Ring Indicator (RI)
Short 1-3 (5V)	Pin 1	Pin 1	Pin 1	Pin 1	Power for 5V
Short 2-4 (12V)	Pin 9	Pin 8	Pin 8	Pin 8	Power for 12V

2.4 Connectors

The onboard connectors link the SBC84500VEA to external devices such as hard disk, floppy disk or printer. The following table lists the function of each connector on the SBC84500VEA. Corresponding pin assignments are described in Chapter 3.

Connector	Description
J1	IrDA Connector
U25	CompactFlash Socket
LCD1	Flat Panel Connector
IDE1	IDE Connector
CON1	Parallel Port
JP6	Power LED
FDD1	FDC Connector
LAN1	Ethernet Connector (1st)
KBMS1	K/B and PS/2 Connector
COM1	COM1
COM2	COM2
COM3	COM3
COM4	COM4
VGA1	CRT Connector
USB1,USB2	USB Connector
J2	Main Power Connector (+5V,+12V)
CN1	8 Bit Digital I/O Connector
PC104-1	PC/104 Connector
PC104-2	PC/104 Connector
SOMIMM1	SODIMM Socket
JP7	HDD LED
JP4	Hardware Reset
JP3	Audio Connector

Chapter 3
Hardware Description

3.1 Safety Precaution

Disconnect the power cord from the SBC84500VEA before your installation. Do not make any connections while the power is on because the sudden surge of power could ruin any sensitive components. Most electronic components are sensitive to the static electric charge. Therefore, before touching the SBC84500VEA control board, always ground yourself to keep from any static charge. Use a grounding wrist strap and place all electronic components in any static-shielded devices.

3.2 CPU

The SBC84500VEA supports an onboard Gx1-233MHz CPU. Systems based on these CPUs can be operated under Linux, Windows NT, Windows 95, 98 and MS-DOS environments. Moreover, the installed CPU determines system's performance.

3.3 BIOS

The system BIOS used in SBC84500VEA is Award Plug and Play BIOS. The SBC84500VEA contains a single 2MB Flash EPROM and supports power-on modification of the system BIOS.

3.4 System Memory

SBC84500VEA has one onboard 144-pin SODIMM sockets, able to support 16MB, 32MB, 64MB, 128MB SODIMM modules, providing the user with up to 128MB system memory.

3.5 Interrupt Controller

The SBC84500VEA is a fully PC compatible control board. It consists of 16 ISA interrupt request lines and 4 of the 16 can be either ISA or PCI. The mapping list of the 16 interrupt request lines is shown below;

NMI	Parity check error
IRQ0	System timer output
IRQ1	Keyboard
IRQ2	Interrupt rerouting from IRQ8 through IRQ15
IRQ3	Serial port #2
IRQ4	Serial port #1
IRQ5	Audio port
IRQ6	Floppy disk controller
IRQ7	Parallel port #1
IRQ8	Real time clock
IRQ9	Reserved
IRQ10	Serial port #3
IRQ11	Serial port #4
IRQ12	PS/2 mouse
IRQ13	Math co-processor
IRQ14	Primary IDE channel
IRQ15	Reserved

3.6 System I/O Address Map

I/O	Address Map Description
000-01F	DMA Controller #1
020-021	Interrupt Controller # 1, Master
022-023	Chipset address
040-05F	System Timer
060-06F	Standard 101/102 keyboard Controller
070-07F	Real time Clock, NMI Controller
080-0BF	DMA Page Register
0A0-0BF	Interrupt Controller # 2
0C0-0DF	DMA Controller # 2
0F0-0FF	Math Coprocessor
170-1FF	VIR BUS Master PCI IDE Controller
220-22F	Audio 16bit sound
2E8-2EF	Serial Port 4
2F8-2FF	Serial Port 2
378-37F	Parallel Printer Port 1
3B0-3DF	Cyrix Graphic Adapter
3E8-3EF	Serial Port 3
3F0-3F7	Floppy Disk Controller
3F8-3FF	Serial Port 1

120 Watch dog timer enable
121 Watch dog timer disable
PNP audio I/O map range from 220~250H (16 bytes)
MPU-401 select from 300~330H (2 bytes)

3.7 DMA channel assignments

Channel	Function
0	Available
1	Available
2	Floppy disk (8-bit transfer)
3	Parallel**
4	Cascade for DMA controller 1
5	Available
6	Available
7	Available

3.8 IDE Interface Connector

The SBC84500VEA builds in 1 channel, able to support 2 IDE drives, PCI bus enhanced IDE controller which can support master/slave mode and post write transaction mechanisms with 64-byte buffer, and master data transaction.

IDE1: IDE Connector Pin Assignment

Pin	Description	Pin	Description
1	Reset #	2	GND
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	GND	20	No connector
21	INPACK	22	GND
23	IOW #	24	GND
25	IOR #	26	GND
27	IOCHRDY	28	GND
29	DACK	30	GND
31	Interrupt IRQ14	32	WP
33	SA1	34	PDIAG
35	SA0	36	SA2
37	HDC CS0 #	38	HDC CSI #
39	HDD Active #	40	No connector
41	+5V	42	+5V
43	GND	44	No connector

3.9 CompactFlash™ Socket (U25)

The SBC84500VEA Series is equipped with a CompactFlash disk socket on the solder side and it supports the IDE interface CompactFlash disk card. The socket itself is especially designed to prevent any incorrect installation of the CompactFlash disk card.
When installing or removing the CompactFlash disk card, please make sure that the system power is off.
The CompactFlash disk card is defaulted as the C: or D: disk drive in your PC system.

3.10 Display Interface

3.10.1 Flat Panel/CRT Interface Controller

The SBC84500VEA builds in CS5530A, a high-performance flat panel/super VGA display controller with onboard 1.5M~4M byte. It is capable to drive CRT display and a wide array of flat panel displays.

Chipset:	NS CX5530A
Display memory:	1 ~ 4 MB share memory, set in BIOS
Display type:	Supports CRT and TFT LCD displays. Can display CRT and flat panel simultaneously
Flat panel display mode:	Panel resolution supports up to 1024 x 768 @ 18 bpp. Supports 18-bit TFT LCD panel
CRT display mode:	Non-interlaced CRT monitors resolutions up to 1280 x 1024 @ 256 colors or 1024 x 768 @ 16 bpp

3.10.2 VGA/Flat Panel Connectors

The SBC84500VEA has two connectors to support the CRT VGA and flat panel displays, respectively or simultaneously. **VGA1** is a standard 15-pin connector commonly used for the CRT VGA display, and **LCD1** is a 44-pin, dual-in-line header for flat panel connection. Configuration of the VGA interface is done via the software utility and no jumper setting is required. The following two tables are the pin assignments for the CRT/VGA connector and the flat panel connector, respectively.

VGA1: CRT/VGA Connector Pin Assignment

Pin	Description	Pin	Description
1	Red	2	Green
3	Blue	4	N/A
5	GND	6	GND
7	GND	8	GND
9	DCC VCC	10	GNS
11	No connector	12	DCC Serial Data
13	Horizontal Sync	14	Vertical Sync
15	DCC Serial Clock	16	No connector

LCD1: Flat Panel Connector Pin Assignment

Pin	Description	Pin	Description
1	No connector	2	+12VM
3	GND	4	GND
5	VDDM	6	VDDM
7	No connector	8	GND
9	No connector	10	No connector
11	B0 (P2)	12	B1 (P3)
13	B2 (P4)	14	B3 (P5)
15	B4 (P6)	16	B5 (P7)
17	No connector	18	No connector
19	G0 (P10)	20	G1 (P11)
21	G2 (P12)	22	G3 (P13)

Continued . . . . .

Pin	Description	Pin	Description
23	G4 (P14)	24	G5 (P15)
25	No connector	26	No connector
27	R0 (P18)	28	R1 (P19)
29	R2 (P20)	30	R3 (P21)
31	R4 (P22)	32	R5 (P23)
33	GND	34	GND
35	FPCLK	36	FPVSYNC (FLM)
37	FPDISP	38	FPHSYNC (LP)
39	GND	40	FPENABKL
41	GND	42	No connector
43	No connector	44	VDDM

3.10.3 Flat Panel Connector Pin Description

Name	Description
P0~P23	Flat panel data output
FPENABKL	Flat Panel Backlight Enable Output
FPCLK	Flat Panel Clock
FPDISP	Flat Panel Display Enable Output
FPVSYNC	Flat Panel Vertical Sync Output
FPHSYNC	Flat Panel Horizontal Sync Output
+12VM	Controlled +12V power
VDDM	Controlled 3.3V or 5V power selected by JP2

3.11 Floppy Disk Controller

The SBC84500VEA provides a 34-pin header type connector, **FDD1** for supporting up to two floppy drives. The floppy drives could be any one of the following types: 3.5" /1.44MB/2.88MB.

FDD1: Floppy Disk Connector Pin Assignment

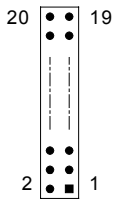
Pin	Description	Pin	Description
1	GND	2	Reduce write current
3	GND	4	No connector
5	GND	6	Density select
7	GND	8	Index #
9	GND	10	Motor enable A #
11	GND	12	Drive select B #
13	GND	14	Drive select A #
15	GND	16	Motor enable B #
17	GND	18	Direction #
19	GND	20	STEP #
21	GND	22	Write data #
23	GND	24	Write gate #
25	GND	26	Track 0 #
27	GND	28	Write protect #
29	NC	30	Read data #
31	GND	32	Head select #
33	NC	34	Disk change #

3.12 Digital I/Os

The board is equipped with a 8-channel digital I/O connector **CN1** that meets a system's customary automation control needs. The digital I/O can be configured to control the cash drawer, or to sense the warning signal of an Uninterrupted Power System (UPS), or to perform the store security control. The digital I/O is controlled via software programming.

CN1: Digital I/O Connector

Pin	Signal	Pin	Signal
1	DIO Out 0	2	DIO In 0
3	DIO Out 1	4	DIO In 1
5	DIO Out 2	6	DIO In 2
7	DIO Out 3	8	DIO In 3
9	DIO Out 4	10	DIO In 4
11	DIO Out 5	12	DIO In 5
13	DIO Out 6	14	DIO In 6
15	DIO Out 7	16	DIO In 7
17	GND	18	GND
19	NC	20	NC



3.12.1 Digital I/O Software Programming

The Digital I/O on the the board is not an isolated type.

Output	Address	Bit	Output	Address	Bit
Out-0	123h	0	In-0	123h	0
Out-1	123h	1	In-1	123h	1
Out-2	123h	2	In-2	123h	2
Out-3	123h	3	In-3	123h	3
Out-4	123h	4	In-4	123h	4
Out-5	123h	5	In-5	123h	5
Out-6	123h	6	In-6	123h	6
Out-7	123h	7	In-7	123h	7

Example program;

Out 123h, 03h	Out-0, Out-1	Turn On
	Out-2, Out-3	Turn Off
Out 123h, 0Ah	Out-0, Out-2	Turn Off
	Out-1, Out-3	Turn On

Example program;

If INPUT 123 is
(1011), then INPUT-2 is "0"
If INPUT 123 is (1100), then INPUT-0 & 1 are "0"
** The INPUT signal has to be TTL signal

3.13 Parallel Port Interface

The onboard PRT of SBC84500VEA is a multi-mode parallel port able to support:

- **Standard mode:** IBM PC/XT, PC/AT and PS/2™ compatible with bi-directional parallel port
- **Enhanced mode:** Enhance parallel port (EPP) compatible with EPP 1.7 and EPP 1.9 (IEEE 1284 compliant)
- **High speed mode:** Microsoft and Hewlett Packard extended capabilities port (ECP) IEEE 1284 compliant

The address select of the onboard parallel port in LPT1 (378H), LPT2 (278H), LPT3 (3BCH) or disabled is done by BIOS CMOS setup.

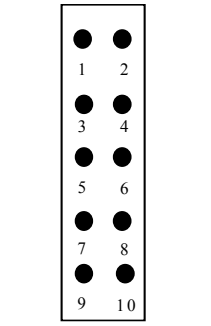
CON1: Parallel Port Connector Pin Assignment

Pin	Description	Pin	Description
1	Strobe #	2	Auto Form Feed #
3	Data 0	4	Error #
5	Data 1	6	Initialize #
7	Data 2	8	Printer Select In #
9	Data 3	10	GND
11	Data 4	12	GND
13	Data 5	14	GND
15	Data 6	16	GND
17	Data 7	18	GND
19	Acknowledge #	20	GND
21	Busy	22	GND
23	Paper Empty #	24	GND
25	Printer Select	26	GND

3.14 Serial Port Interface

The SBC84500VEA has four onboard serial ports, with COM1,COM3,COM4 as RS-232 and COM2 as RS-232/422/485, both selected via jumper setting. Both ports have +5V/12V power on pins 1 (+5V) and 8 or pin 9 (+12V), depending on jumper selection. The RS-232's pin assignments are listed below;

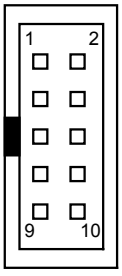
CON1	COM2	COM3	COM4	Description
1	1	1	1	Data Carrier Detect (DCD)
6	2	2	2	Data Set Ready (DSR)
2	3	3	3	Receive Data (RXD)
7	4	4	4	Request to Send (RTS)
3	5	5	5	Transmit Data (TXD)
8	6	6	6	Clear to Send (CTS)
4	7	7	7	Data Terminal Ready (DTR)
9	8	8	8	Ring Indicator (RI)
5	9	9	9	Ground (GND)
X	10	10	10	GND



NOTE: *The COM2~COM4 ports of SBC84500VEA are pin header type connectors and COM1 is a DB-9 connector.*

The RS-422/485 pin assignment for COM2 is listed as follows;

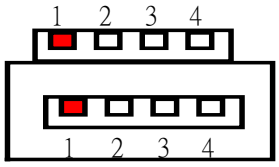
Pin	RS-422	RS-485
1	TXD-	DATA-
2	x	X
3	TXD+	DATA+
4	x	X
5	RXD+	X
6	x	X
7	RXD-	X
8	x	X
9	GND	GND
10	x	X



3.15 USB Connector

There are two USB connectors allow installation of USB devices. USB1 is a single standard USB connector. USB1 is 4-pin header connector. The following table shows the pin outs of the USB connector.

Pin #	Signal Name
1	USB0/1 Vcc
2	USB0/1-
3	USB0/1+
4	USB0/1 GND

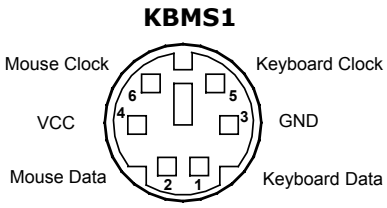


3.16 Real Time Clock and CMOS RAM

The SBC84500VEA contains an MC146818 compatible Real Time Clock (RTC) and 128 byte of CMOS RAM in the WINBOND W83977AF, or its equivalent. The CMOS RAM stores the system configuration information entered via the SETUP program. The RTC and the CMOS RAM are kept active by a battery when the system power is turned off, and the battery power can last for ten years.

3.17 Keyboard and PS/2 Mouse Connector

KBMS1 is a DIN connector for PS/2 keyboard connection.

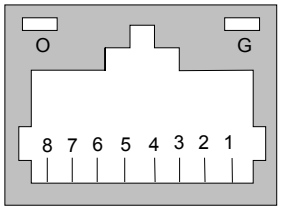


3.18 Ethernet Connector

The RJ-45 connector (**Lan1**) is used for Ethernet. To connect the SBC84500VEA to a hub, just plug one end of the cable into the **Lan1** and connect the other end of the cable to a hub.

LAN1 : RJ-45 Connector Pin Assignment

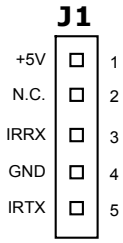
Pin	Signal
1	Tx+ (Data transmission positive)
2	Tx- (Data transmission negative)
3	Rx+(Data reception positive)
6	Rx- (Data reception negative)
other	Not use
G	Green LED, light when 100M link
O	Orange LED,flash when active



RJ-45

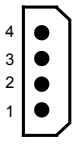
3.19 IrDA Connector

J1 is a 5-pin IrDA connector for wireless communication.



3.20 Power Input Connectors

J2 is the +5V/+12V power input connector of the SBC84500VEA. The SBC84500VEA needs +5V for normal operation.



Pin	Description
1	+12V
2	GND
3	GND
4	+5V

3.21 PC/104 Connectors

The PC/104 is an industrial standard. It is a compact form factor of the dimension of 3.6" x 3.8" and is fully compatible with the ISA Bus. The PC/104 interface is able to adapt the off-shelf PC/104 modules, such as sound module, fax modem module and multi-I/O module…etc.

PC104-1: PC/104 Bus Pin Assignment

PIN No.	PIN Name	PIN No.	PIN Name
1	IOCHCHK *	2	GND
3	SD7	4	RESETDRV
5	SD6	6	+5V
7	SD5	8	IRQ9
9	SD4	10	NC
11	SD3	12	DRQ2
13	SD2	14	NC
15	SD1	16	ZEROWS*
17	SD0	18	+12V
19	IOCHRDY	20	GND
21	AEN	22	SMEMW *
23	SA19	24	SMEMR *
25	SA18	26	IOW *
27	SA17	28	IOR *
29	SA16	30	DACK3 *
31	SA15	32	DRQ3
33	SA14	34	DACK1 *
35	SA13	36	DRQ1
37	SA12	38	REFRESH *
39	SA11	40	SYSCLK
41	SA10	42	IRQ7
43	SA9	44	IRQ6
45	SA8	46	IRQ5
47	SA7	48	IRQ4

Continued . . . . .

PIN No.	PIN Name
49	SA6
51	SA5
53	SA4
55	SA3
57	SA2
59	SA1
61	SA0
63	GND

PIN No.	PIN Name
50	IRQ3
52	DACK2 *
54	TC
56	SALE
58	+5V
60	OSC
62	GND
64	GND

PC104-2: PC/104 Bus Pin Assignments

PIN No.	PIN Name
1	GND
3	MEMCS16 *
5	IOCS16 *
7	IRQ10
9	IRQ11
11	IRQ12
13	IRQ15
15	IRQ14
17	DACK0 *
19	DRQ0
21	DACK5 *
23	DRQ5
25	DACK6 *
27	DRQ6
29	DACK7 *
31	DRQ7
33	+5V
35	MASTER *
37	GND
39	GND

PIN No.	PIN Name
2	GND
4	SBHE *
6	LA23
8	LA22
10	LA21
12	LA20
14	LA19
16	LA18
18	LA17
20	MEMR *
22	MEMW *
24	SD8
26	SD9
28	SD10
30	SD11
32	SD12
34	SD13
36	SD14
38	SD15
40	NC

3.22 HDD LED Connector

JP7: 2 Pin connector for HDD LED communication.

Pin	Description
1	LED+
2	LED-

3.23 Power LED Connector

JP6: 2 Pin connector for Power LED communication.

Pin	Description
1	LED+
2	LED-

3.24 Hardware Reset Connector

JP4: 2 Pin connector for Hardware Reset communication.

Pin	Description
1	Signal
2	GND

3.25 Audio Connector

JP3: 10 Pin connector for Audio communication.

Pin	Description
1	Mic Signal
3	Left Line Input Signal
5	Right Line Input Signal
7	Left Audio Output Signal
9	Right Audio Output Signal
2,4,6,8,10	GND

Chapter 4
Display Drivers

4.1 Introduction

The SBC84500VEA Series has an on-board LCD/VGA interface. The specifications and features are described as follows:

4.1.1 Chipset

The SBC84500VEA uses a NS CS5530A chipset for its SVGA controller. It supports many popular 18-bit LCD displays and conventional analog CRT monitors. The VGA BIOS supports LCD. In addition, it also supports interlaced and non-interlaced analog monitors (color and monochrome VGA) in high-resolution modes while maintaining complete IBM VGA compatibility.

4.1.2 Display memory

With 1 ~ 4 MB share memory, the VGA controller can drive CRT displays or color panel displays with resolutions up to 1024 x 768 at 64 K colors. The display memory can be expanded to 4 MB in BIOS for true-color resolution of 1024 x 768.

4.2 Installation of SVGA driver

Complete the following steps to install the SVGA driver. Follow the procedures in the flow chart that apply to the operating system that you are using within your SBC84500.

Important: The following windows illustrations are examples only. You must follow the flow chart instructions and pay attention to the instructions which then appear on your screen.

Note 1:

The CD-ROM drive is designated as "D:" throughout this chapter.

Note 2:

<Enter> means pressing the "Enter" key on the keyboard.

Note 3:

When you are using a CRT display, please make sure that your flat panel resolution settings (in the BIOS setup) are the same as your VGA resolution settings (in Windows). Otherwise your display may behave strangely.

4.2.1 Installation for National MediaGX Certified drivers for Windows 95/98.

Insert the disk into the CD-ROM drive.

1. Select "Start" then "Run".
   Type the correct path for the driver (like the example below)
   "D:\SBC84500\Win9X\"
   Click "OK"

4.2.2 Display drivers

1. Win95, 98 drivers (VGA & Audio) in \Win9X\National Geode Win9x Drivers 1.2
2. WinNT4.0 drivers in \NT4.0 Display Driver 5.05

Chapter 5
Ethernet Introduction

5.1 Introduction

The SBC84500VEA is equipped with a high performance Plug and Play Ethernet interface which is fully compliant with the IEEE 802.3 standard, and consisting of a RJ-45 connector **Lan1**.

5.2 Features

- 10Mb/s and 100Mb/s operations
- Supports 10Mb/s and 100Mb/s N-Way auto negotiation
- Full duplex capability
- Full compliance with PCI Revision 2.1
- PCI Bus Master data transfers

5.3 Drivers Supported

Bundled with popular software drivers, the SBC84500VEA Ethernet interface allows great flexibility to work with all major networking operating systems including Novell NetWare v2.x, v3.x, v4.x, Microsoft LAN Manager, Win3.1, Win NT, Win95, IBM LAN Server, SCO UNIX or other ODI, NDIS and Packet drive compliant operating systems.

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Chapter 6
Award BIOS Utility

This chapter describes the different settings available in the Award BIOS that comes with the SBC84500VEA CPU card. Also contained here are instructions on how to set up the BIOS configuration.

6.1 System test and initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors. Non-fatal error messages usually appear on the screen along with the following instructions:

press <F1> to RESUME

Write down the message and press the F1 key to continue the bootup sequence.

6.1.1 System configuration verification

These routines check the current system configuration against the values stored in the board's CMOS memory. If they do not match, the program outputs an error message. You will then need to run the BIOS setup program to set the configuration information in memory. There are three situations in which you will need to change the CMOS settings:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The CMOS memory has lost power and the configuration information has been erased.

The SBC84500 Series' CMOS memory has an integral lithium battery backup. The battery backup should last ten years in normal service, but when it finally runs down, you will need to replace the complete unit.

6.2 Award BIOS setup

Award's BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM so that it retains the Setup information when the power is turned off.

6.2.1 Entering setup

Power on the computer and press <Del> immediately. This will allow you to enter Setup.

ROM PCI/ISA BIOS (SBC84500)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP	INTEGRATED PERIPHERALS
BIOS FEATURES SETUP	SUPERVISOR PASSWORD
CHIPSET FEATURES SETUP	USER PASSWORD
POWER MANAGEMENT SETUP	IDE HDD AUTO DETECTION
PNP/PCI CONFIGURATION	SAVE & EXIT SETUP
LOAD BIOS DEFAULTS	EXIT WITHOUT SAVING
LOAD SETUP DEFAULTS	
Esc : Quit	↑↓→← : Select Item
F10 : Save & Exit Setup	(Shift) F2 : Change Color

6.2.2 Standard CMOS setup

The Standard CMOS Setup is used for basic hardware system configuration. The main function is for Date/Time setting and Floppy/Hard Disk Drive setting. Please refer the following screen for this setup.

ROM PCI/ISA BIOS (SBC84500)
STANDARD CMOS SETUP
AWARD SOFTWARE, INC.

Date (mm:dd:yy) : Thu, May 24 2001

Time (hh:mm:ss) : 13 : 24 : 7

		CYLS.	HEADS	PRECOMP	LANDZONE	SECTORS	MODE
Drive C	: 0 (0Mb)	0	0	0	0	0	AUTO
Drive D	: 0 (0Mb)	0	0	0	0	0	AUTO

Drive A : 1.44M, 3.5in
Drive B : None

Video : EGA / VGA

Halt On : All, But Keyboard

ESC : Quit
F1 : Help

↑ ↓ → ← : Select Item PU / PD / + / - : Modify
(Shift) F2 : Change Color

- **To set the Date:** for example, press either the arrow or <Enter> button on your keyboard to select one of the fields (Month, Date or Year) then press either <PgUp> or <PgDn> to increase or decrease the value of that field. Do the same steps for Time setting.
- **For IDE hard disk drive setup:** please check the following possible setup procedure:

  1. Use the Auto setting for detection during boot-up.
  2. Use the IDE HDD AUTO DETECTION in the main menu; the computer will automatically detect the HDD specifications.
  3. Manually enter the specifications by yourself from the "User" option.

  Note: If you need more information on any particular field, just highlight it then press <F1> button. A pop-up window will come out to give you more information on that field.

6.2.3 BIOS features setup

This BIOS Features Setup is designed for the 'fine tuning' of your system in order to improve its performance. As for normal operation, you don't have to change any default setting. The default setting is pre-set for most reliable operation.

ROM PCI/ISA BIOS (SBC84500)
BIOS FEATURES SETUP
AWARD SOFTWARE, INC.

Virus Warning	: Disabled	Video BIOS Shadow	: Enabled
CPU Internal Cache	: Enabled	C8000-CBFFF Shadow	: Disabled
		CC000-CFFFF Shadow	: Disabled
Quick Power On Self Test	: Enabled	D0000-D3FFF Shadow	: Disabled
Boot Sequence	: C, A, SCSI	D4000-D7FFF Shadow	: Disabled
Swap Floppy Drive	: Disabled	D8000-DBFFF Shadow	: Disabled
Boot Up Floppy Seek	: Disabled	DC000-DFFFF Shadow	: Enabled
Boot Up NumLock Status	: On	Cyrix 6x86/MII CPUID	: Enabled
Boot Up System Speed	: High		
Gate A20 Option	: Fast		
Memory Parity Check	: Enabled		
Typematic Rate Setting	: Disabled		
Typematic Rate (Chars/Sec)	: 6		
Typematic Delay (Msec)	: 250		
Security Option	: Setup	ESC : Quit	↑ ↓ → ←: Select Item
PS/2 mouse function control	: Enabled	F1 : Help	PU/PD/+/- : Modify
PCI/VGA Palette Snoop	: Disabled	F5 : Old Values	(Shift) F2 : Color
OS Select For DRAM > 64MB	: Non-OS2	F6 : Load BIOS Defaults	
Report No FDD For WIN 95	: Yes	F7 : Load Setup Defaults	

6.2.4 Chipset features setup

This setup function works mostly on board's chipset. This option is used to change the chipset's configuration. Please, carefully change any default setting, otherwise the system will run unstable.

ROM PCI/ISA BIOS (SBC84500)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

SDRAM CAS lantency TIme	: 3 T	
SDRAM Clock Ratio Div By	: 4	
16-bit I/O Recovery (CLK)	: 5	
8-bit I/O Recovery (CLK)	: 5	
USB Controller	: Enabled	
USB Legacy Support	: Disabled	
		ESC : Quit ↑↓→←: Select Item F1 : Help PU/PD/+/- : Modify F5 : Old Values (Shift) F2 : Color F6 : Load BIOS Defaults F7 : Load Setup Defaults

6.2.5 Power management setup

Power Management Setup helps user to handle the SBC84500 board's "green" function. This feature can shut down the video display and hard disk to save energy, for example. The power management setup screen is as following.

ROM PCI/ISA BIOS (SBC84500)
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC.

Power Management	: Disabled	IRQ1	(KeyBoard)	: ON
	: 4	IRQ3	(COM 2)	: OFF
** PM Timers **		IRQ4	(COM 1)	: OFF
Doze Mode	: Disabled	IRQ5	(LPT 2)	: OFF
Standby Mode	: Disabled	IRQ6	(Floppy Disk)	: OFF
HDD Power Down	: Disabled	IRQ7	(LPT 1)	: OFF
MODEM Use IRQ	: NA	IRQ9	(IRQ2 Redir)	: OFF
		IRQ10	(Reserved)	: OFF
Throttle Duty Cycle	: 33.3%	IRQ11	(Reserved)	: OFF
		IRQ12	(PS/2 Mouse)	: OFF
		IRQ13	(Coprocessor)	: OFF
		IRQ14	(Hard Disk)	: OFF
		IRQ15	(Reserved)	: OFF

ESC :	Quit	↑↓→←:	Select Item
F1 :	Help	PU/PD/+/- :	Modify
F5 :	Old Values	(Shift) F2 :	Color
F6 :	Load BIOS Defaults		
F7 :	Load Setup Defaults		

6.2.6 PnP/PCI configuration

This menu is used to assign certain IRQ to your PNP/PCI Devices manually.

ROM PCI/ISA BIOS (SBC84500)
PNP/PCI CONFIGURATION
AWARD SOFTWARE, INC.

PNP OS Installed	: No	PCI IRQ Actived By :	Level
Resources Controlled By	: Auto		
Reset Configuration Data	: Disabled		
		OnBoard EtherNet BootROM:	Disabled
		ESC : Quit	↑↓→←: Select Item
		F1 : Help	PU/PD/+/- : Modify
		F5 : Old Values	(Shift) F2 : Color
		F6 : Load BIOS Defaults	
		F7 : Load Setup Defaults	

- **PNP OS Installed:** if you install Plug and Play operating system (OS), the OS will reassign the interrupt if you select *Yes* in this field. If you install a non-Plug and Play OS or if you want to prevent reassigning of interrupt settings, select *No* in this field.
- **Resources Controlled By:** select *Auto* if you want the computer to assign the IRQs automatically and vice versa.
- **Reset Configuration Data:** *Enabling* this field means you allow the configuration data to be reset.
- **IRQ-xx assigned to:** these fields show whether a PCI/ISA uses certain IRQ.

6.2.7 Integrated peripherals

By choosing the INTEGRATED PERIPHERALS option from the INITIAL SETUP SCREEN menu, the screen below is displayed. This sample screen contains the manufacturer's default values for the SBC84500VEA Series. The PANEL TYPE by default supports a 18-bit 640 x 480 TFT LCD panel display.

ROM PCI/ISA BIOS (SBC84500)
INTEGRATED PERIPHERALS
AWARD SOFTWARE, INC.

IDE HDD Block Mode	: Enabled	Onboard Serial Port 3	: 3E8H
Primary IDE Channel	: Enabled	Serial Port 3 Use IRQ	: IRQ10
Master Drive PIO Mode	: Auto	Onboard Serial Port 4	: 2E8H
Slave Drive PIO Mode	: Auto	Serial Port 4 Use IRQ	: IRQ11
IDE Primary Master UDMA	: Auto	Build in CPU Audio	: Enabled
IDE Primary Slave UDMA	: Auto	Audio I/O Base Address	: 220H
KBC input clock	: 8 MHz	MPU-401 I/O Base Address	: 330H
Onboard FDC Controller	: Enabled	Audio IRQ Select	: IRQ5
Onboard Serial Port 1	: 3F8/IRQ4	Audio Low DMA Select	: DMA 1
Onboard Serial Port 2	: 2F8/IRQ3	Audio High DMA Select	: DMA 5
Onboard IR Controller	:	Video Memory Size	: 2.5 M
IR Address Select	: 3E0H	Display status	: Both
IR Mode	:	Flat Panel Resolution	: 640x480
IR Transmission delay	: Enabled		
IR IRQ Select	:		
IR Mode Use DMA	: Disable	ESC : Quit	↑↓→←: Select Item
Onboard Parallel Port	:	F1 : Help	PU/PD/+/- : Modify
Parallel Port Mode	:	F5 : Old Values	(Shift) F2 : Color
ECP Mode Use DMA	:	F6 : Load BIOS Defaults	
EPP Mode Select	: EPP1.9	F7 : Load Setup Defaults	

This option is used to assign Onboard I/O, IRQ, and DMA etc. If you don't know how to configure them, just press <F7> to load Setup Defaults. The flat panels will then be applied with two modes: 640x480 r 800x600, for which it needs to set up from BIOS for proper flat panel resolution.

- **Build in CPU Audio -- Enabled, Disabled**

  To disable/enable the audio function.

- **Audio I/O Base Address -- 220H, 240H, 260H, 280H**

  To select the I/O address for audio function.

- **MPU-401 I/O Base Address -- 300H, 330H, Disabled**

  To select the I/O address for MPU-401 (midi interface).

- **Audio IRQ Select -- 5, 7, 10, Disabled**

  To select the interrupt for audio function.

- **Audio Low DMA Select -- DMA0, DMA1, DMA3, Disabled**

  To select the high DMA channel.

- **Audio High DMA Select -- DMA5, DMA6, DMA7, Disabled**

  To select the high DMA channel.

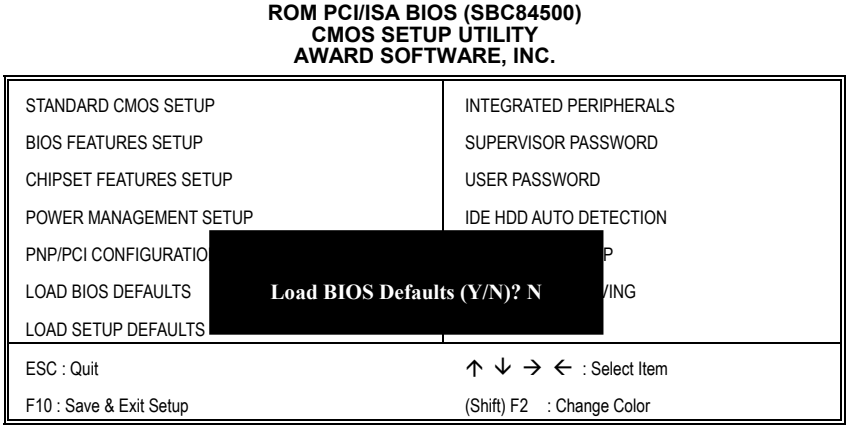
- **Video Memory Size -- 1.5M, 2.5M, 4.0M**

  To select the size of video memory. It makes use of system memory for display.

6.2.8 Load BIOS defaults

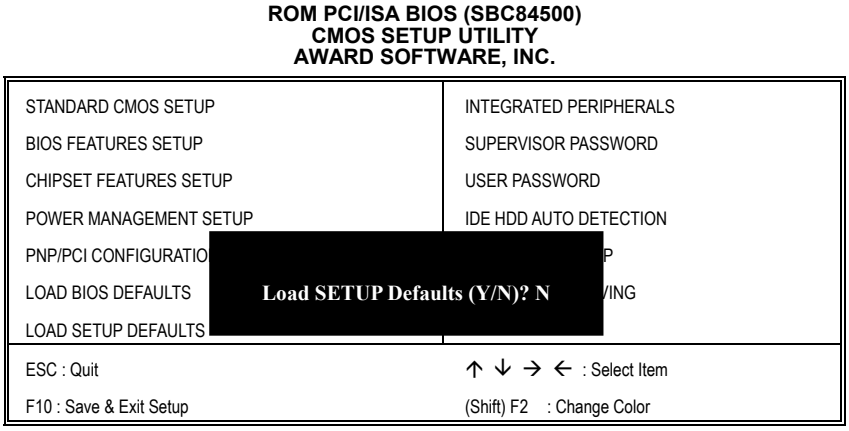
If you select 'Y' to this field, the BIOS Defaults will be loaded except Standard CMOS SETUP. The default settings are not optimal and turning all high performance into disabled condition. Select 'N' to abort.

Suggestion: for the first time or for our primary user, we suggest you to use LOAD SETUP DEFAULTS because it is the safest mode for your system.



6.2.9 LOAD SETUP DEFAULTS

If you select 'Y' to this field, the Setup Defaults will be loaded except Standard CMOS SETUP. The default settings are optimal configuration settings for your system.



6.2.10 Change password

To change the password, choose the PASSWORD SETTING option form the Setup main menu and press <Enter>.

1. If the CMOS is bad or this option has never been used, a default password is stored in the ROM. The screen will display the following messages:

   Enter Password:

   Press <Enter>.
2. If the CMOS is good or this option has been used to change the default password, the user is asked for the password stored in the CMOS. The screen will display the following message:

   Confirm Password:

   Enter the current password and press <Enter>.
3. After pressing <Enter> (ROM password) or the current password (user-defined), you can change the password stored in the CMOS. The password can be at most eight (8) characters long. Remember - to enable this feature, you must first select either Setup or System in the BIOS FEATURES SETUP.

6.2.11 Auto detect hard disk

This option detects the parameters of an IDE hard disk drive (HDD sector, cylinder, head, etc) automatically and will put the parameters into the Standard CMOS Setup screen. Up to 2 IDE drives can be detected and the parameters will be listed in the box. Press <Y> if you accept these parameters. Press <N> to skip the next IDE drives.

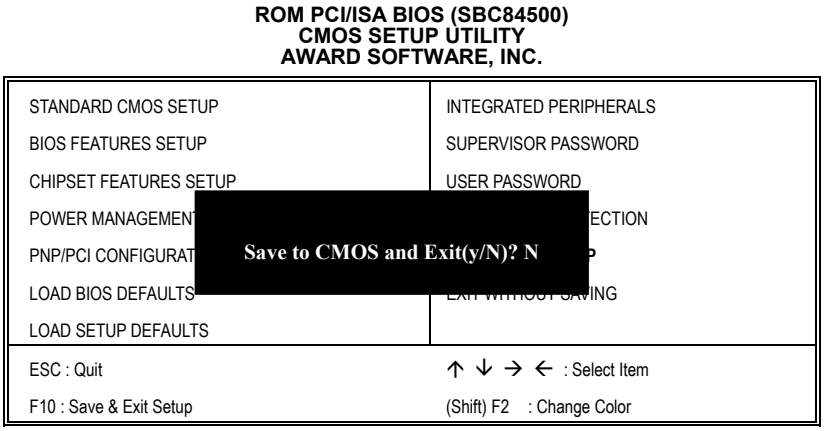
ROM PCI/ISA BIOS (SBC84500)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP	INTEGRATED PERIPHERALS
BIOS FEATURES SETUP	SUPERVISOR PASSWORD
CHIPSET FEATURES SETUP	USER PASSWORD
POWER MANAGEMENT SETUP	IDE HDD AUTO DETECTION
PNP/PCI CONFIGURATION	TUP
LOAD BIOS DEFAULTS	AVING
LOAD SETUP DEFAULTS	
ESC : Quit	↑ ↓ → ← : Select Item
F10 : Save & Exit Setup	(Shift) F2 : Change Color

NOT AVAILABLE in DOS Version !

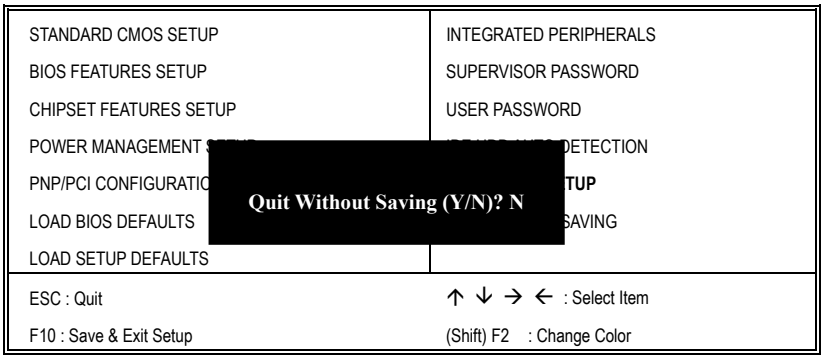
6.2.12 Save & exit setup

If you select this option and press <Enter>, the values entered in the setup utilities will be recorded in the chipset's CMOS memory. The microprocessor will check this every time you turn your system on and compare this to what it finds as it checks the system. This record is required for the system to operate.



6.2.13 Exit without saving

Selecting this option and pressing <Enter> lets you exit the Setup program without recording any new values or changing old ones.



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Appendix A
Watchdog Timer

Using the Watchdog Function

The SBC84500VEA CPU card uses version 2.0 of the watchdog timer. This onboard WDT generates either a system reset , depending on the settings made on jumper **JP1** of SBC84500VEA. Follow the steps below to enable and program the watchdog function of SBC84500VEA.

Start
↓

Un-Lock WDT	:	**OUT 120H 0AH ; enter WDT function** **OUT 120H 0BH ; enable WDT function**
↓		
Set multiple (1~4)	:	**OUT 120 0NH ; N=1,2,3 or 4**
↓		
Set base timer (0~F)	:	**OUT 121 0MH ; M=0,1,2,…F**
↓		
WDT counting		
↓		
re-set timer	:	**OUT 121 0MH ; M=0,1,2,…F**
↓		
IF No re-set timer	:	**WDT time-out, generate RESET**
↓		
IF to disable WDT	:	**OUT 120 00H ; Can be disable at any time**

M	N			
	1	2	3	4
0	0.5 sec.	5 secs.	50 secs.	100 secs.
1	1 sec.	10 secs.	100 secs.	200 secs.
2	1.5 secs.	15 secs.	150 secs.	300 secs.
3	2 secs.	20 secs.	200 secs.	400 secs.
4	2.5 secs.	25 secs.	250 secs.	500 secs.
5	3 secs.	30 secs.	300 secs.	600 secs.
6	3.5 secs.	35 secs.	350 secs.	700 secs.
7	4 secs.	40 secs.	400 secs.	800 secs.
8	4.5 secs.	45 secs.	450 secs.	900 secs.
9	5 secs.	50 secs.	500 secs.	1000 secs.
A	5.5 secs.	55 secs.	550 secs.	1100 secs.
B	6 secs.	60 secs.	600 secs.	1200 secs.
C	6.5 secs.	65 secs.	650 secs.	1300 secs.
D	7 secs.	70 secs.	700 secs.	1400 secs.
E	7.5 secs.	75 secs.	750 secs.	1500 secs.
F	8 secs.	80 secs.	800 secs.	1600 secs.

Appendix B

Electrical Power Requirements

1.Subject :

To measure the CPU power consumption of GX1-233 and 300MHZ.

2.Configuration:

	Windows 98 SE
SDRAM	NEC 128MB(SODIMM)
CPU Usage	100%(GX1-233Mhz)
Memory Usage	>80%
Active Devices	Lan, Video, Audio, COM1~COM4, LPT, IDE, FDD

3.Test condition:

(1)room temp (2)Maxpow ,Windows98

4. SBC84500 Test Result Summary:

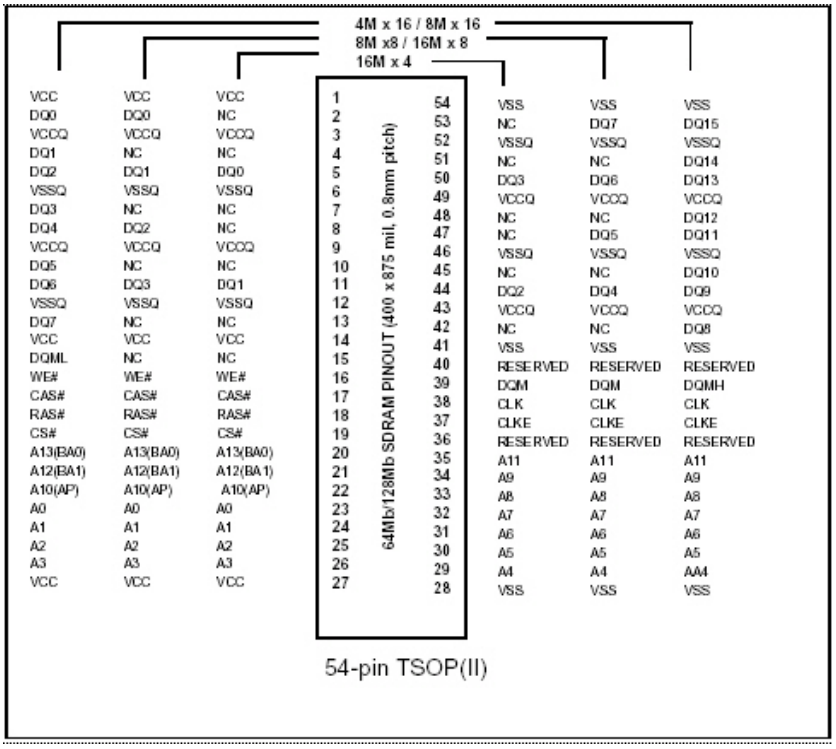
Item	Amp(a)	Pow(w)	Suggest Power Supply (Min Watt)
GX1-233MHZ	1.31A	6.55W	9.17W(min)
GX1-300MHZ	1.54A	7.7W	10.78W(min)

This page does not contain any information.

Appendix C

SO-DIMM Used Notice

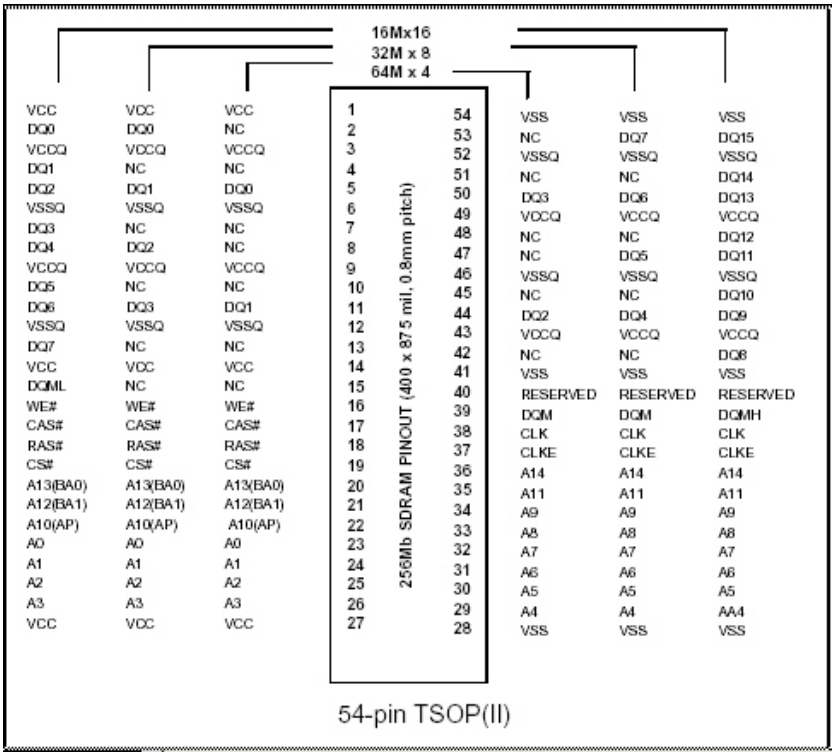
1.PC SDRAM specification overview



SDRAM (4Mx16, 8Mx16, 8Mx8, 16Mx8, 16Mx4 chips Package)

memory address from A0 to A13 total 128M/bit support

(SBC84500 can use)



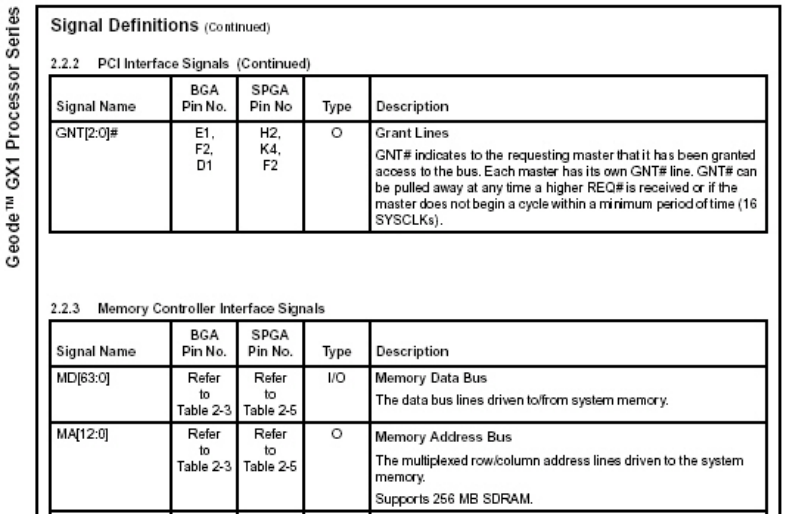
VCC	VCC	VCC	1		54	VSS	VSS	VSS
DQ0	DQ0	NC	2		53	NC	DQ7	DQ15
VCCQ	VCCQ	VCCQ	3		52	VSSQ	VSSQ	VSSQ
DQ1	NC	NC	4		51	NC	NC	DQ14
DQ2	DQ1	DQ0	5		50	DQ3	DQ6	DQ13
VSSQ	VSSQ	VSSQ	6		49	VCCQ	VCCQ	VCCQ
DQ3	NC	NC	7		48	NC	NC	DQ12
DQ4	DQ2	NC	8		47	NC	DQ5	DQ11
VCCQ	VCCQ	VCCQ	9		46	VSSQ	VSSQ	VSSQ
DQ5	NC	NC	10		45	NC	NC	DQ10
DQ6	DQ3	DQ1	11		44	DQ2	DQ4	DQ9
VSSQ	VSSQ	VSSQ	12		43	VCCQ	VCCQ	VCCQ
DQ7	NC	NC	13		42	NC	NC	DQ8
VCC	VCC	VCC	14		41	VSS	VSS	VSS
DQML	NC	NC	15		40	RESERVED	RESERVED	RESERVED
WE#	WE#	WE#	16		39	DQM	DQM	DQMH
CAS#	CAS#	CAS#	17		38	CLK	CLK	CLK
RAS#	RAS#	RAS#	18		37	CLKE	CLKE	CLKE
CS#	CS#	CS#	19		36	A14	A14	A14
A13(BA0)	A13(BA0)	A13(BA0)	20		35	A11	A11	A11
A12(BA1)	A12(BA1)	A12(BA1)	21		34	A9	A9	A9
A10(AP)	A10(AP)	A10(AP)	22		33	A8	A8	A8
A0	A0	A0	23		32	A7	A7	A7
A1	A1	A1	24		31	A6	A6	A6
A2	A2	A2	25		30	A5	A5	A5
A3	A3	A3	26		29	A4	A4	AA4
VCC	VCC	VCC	27		28	VSS	VSS	VSS

SDRAM (16Mx16, 32Mx8, 64Mx4 chips Package)

memory address from A0 to A14 total 256M/bit support

(SBC84500 didn't have address A14, only can detect only 128MB)

2.SBC84500 specification overview



Geode™ GX1 Processor Series

Signal Definitions (Continued)

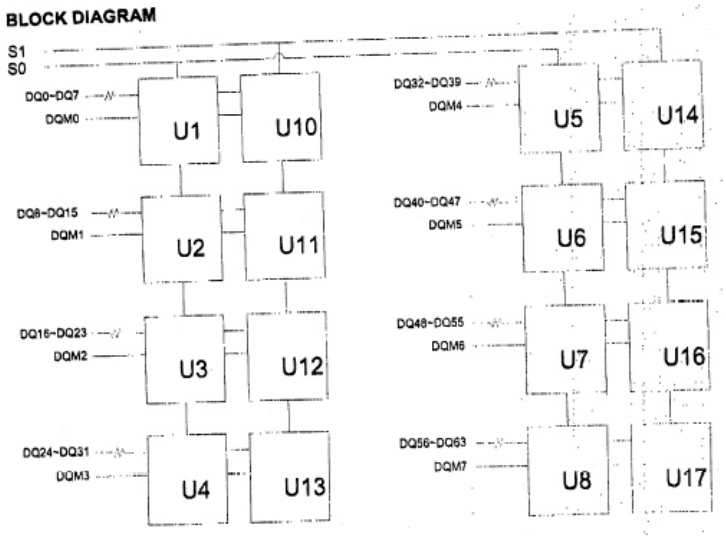
2.2.2 PCI Interface Signals (Continued)

Signal Name	BGA Pin No.	SPGA Pin No	Type	Description
GNT[2:0]#	E1, F2, D1	H2, K4, F2	O	Grant Lines GNT# indicates to the requesting master that it has been granted access to the bus. Each master has its own GNT# line. GNT# can be pulled away at any time a higher REQ# is received or if the master does not begin a cycle within a minimum period of time (16 SYSCLKs).

2.2.3 Memory Controller Interface Signals

Signal Name	BGA Pin No.	SPGA Pin No.	Type	Description
MD[63:0]	Refer to Table 2-3	Refer to Table 2-5	I/O	Memory Data Bus The data bus lines driven to/from system memory.
MA[12:0]	Refer to Table 2-3	Refer to Table 2-5	O	Memory Address Bus The multiplexed row/column address lines driven to the system memory. Supports 256 MB SDRAM.

1. memory address from A0 to A12 , SDRAM (4Mx16,8Mx16,8Mx8,16Mx8,16Mx4 chips Package)
2. total 256M/byte support ,you can use (**Sixteen** CMOS **16Mx8bit** with 4banks SDRAMS or **Sixteen** CMOS **8Mx16bit** with 4banks SDRAMS or **Thirty-two** CMOS **4Mx16bit** with 4banks SDRAMS or **Thirty-two** CMOS **8Mx8bit** with 4banks SDRAMS or **Thirty-two** CMOS **16Mx4bit** with 4banks SDRAMS)on PC SODIMM
3. In really design usually use **Sixteen** CMOS **16Mx8bit** with 4banks SDRAMS or **Sixteen** CMOS **8Mx16bit** with 4banks SDRAMS in TSOP-II package, double side component, six layers foe example like below.



(SODIMM TOP side)

(SODIMM Bottom side)